PATENT

#9 Brief 3/4/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Shields & Ko

Assignee: Advanced Micro Devices, Inc.

Title: A SACRIFICIAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT

Serial No.: 09/208,325 Filed: 12/9/98

Examiner: T. Nguyen Group Art Unit:2813

Attorney Docket No.: D730(HDN1068)

Anthem, Arizona
February 13, 2001

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

BRIEF ON APPEAL

Sir:

This appeal brief is submitted pursuant the Notice of Appeal filed 12/13/00 for the above-identified application.

REAL PARTY IN INTEREST

The real party in interest is ADVANCED MICRO DEVICES, INC.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

The application as filed included Claims 1 – 5. The Examiner in an Office Action dated 4/6/00 rejected Claims 1 – 5. The Applicants filed an amendment dated 7/3/00 amending Claims 1 and 3 and canceling Claim 2. In an Office Action designated as final, dated 9/14/00, the Examiner rejected Claims 1 and 3 – 5. The Applicants, in an Amendment After Final dated 11/17/00, proposed amendments of Claims 1 and 5. The Examiner in an Advisory Action dated 12/6/00 advised that the Amendment After Final would not be entered because the amendments raise new issues that would require further consideration and/or search stating that: "The new limitation 'simultaneously' in claim 1 contain the new subject matter that would require further consideration/search." The Examiner

stated that: "For purposes of Appeal, the status of the claim is that: Claims rejected are 1 and 3 – 5." Appellants therefore understand that the Claims on Appeal are the Claims as presented in the Amendment filed on 7/3/00.

STATUS OF AMENDMENTS

An Amendment After Final dated 11/17/00 was filed in response to the Final Office Action dated 9/14/00. The Applicants proposed amendments of Claims 1 and 5 that narrowed Claims 1 and 5, however the Examiner in an Advisory Action dated 12/6/00 advised that the "new limitation 'simultaneously' in claim 1 contains the new subject matter that would require further consideration/search." The Examiner in the Advisory Action dated 12/6/00 also advised that the "proposed amendment would not be entered because they raise new issues that would require further consideration and/or search." Accordingly, Applicants understand that the Claims under Appeal are the Claims presented in the Amendment dated 7/3/00. A copy of the claims under appeal is in the Appendix.

SUMMARY OF THE INVENTION

The present invention is directed to a method of manufacturing a semiconductor wafer wherein a final layer of metal **104 (Figure 1A)[A copy of the Figures for the present invention is in the Appendix]** is formed on a layer **102** of interlayer dielectric with a layer **106** of TiN formed on the layer **104** and a layer **108** of photoresist formed on the layer **104**. The layer **108** of photoresist is patterned and developed to expose portions of the layer **106** of TiN **(Figure 1B)**. The exposed portions of the layer **106** are etched exposing portions of the layer **104** of metal **(Figure 1C)**. The exposed portions of the layer **104** are etched down to the layer **102** of interlayer dielectric **(Figure 1D)**. The remaining portions of the layer **108** and the layer **106** of TiN are removed entirely **(Figure 2B)** during the same process **(Specification, page 5, lines 28 & 29)**. Because the layer **106** of TiN is removed completely during the same process as the layer **108** of photoresist is stripped it is not necessary to etch the TiN layer during pad etch thus increasing throughput and substantial savings in manufacturing costs. The necessity of stripping the TiN layer during pad etch has decreased throughput in prior art manufacturing methods.

ISSUES

1. Is the rejection of Claim 1 under 35 U.S.C. §102 (e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026) proper?

2. Is the rejection of Claims 1 and 3 – 5 under 35 U.S.C. §103 (a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art proper?

3. Was it proper for the Examiner to refuse to enter the proposed amendment on the ground that the "new limitation 'simultaneously' in claim 1 contain the new subject matter that would require further consideration/search" in view of the fact that the specification contains the language: "The layer **108** of photoresist and the layer **106** of TiN are stripped during the same process step."

GROUPING OF CLAIMS

All of the rejected claims have been grouped together in the Advisory Action dated 12/6/00. Appellants submit that each of the rejected claims stand on its own recitation, the claims being considered to be separately patentable as set forth in more detail below.

THE REFERENCES

Applicants' Admitted Prior Art

Xing et al. U.S. Patent No. 5,880,026 Issued 3/9/99

THE REJECTIONS AND ARGUMENTS

[In the following discussion, the Examiner's specific statements are in normal type, Appellants' comments that immediately follow portions of the Examiner's specific statements are enclosed within brackets "[ ]" and are in bold type.]

ISSUE 1. Is the rejection of Claim 1 under 35 U.S.C. §102 (e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026) proper?

The Examiner rejected Claim 1 under 35 U.S.C. 102(e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026). The Examiner stated that:

> Referring to figures 1-3D, Xing et al. teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) **[This statement is incorrect and indicates that the Examiner does not understand the teachings of Xing et al. Layer 210 is a layer of metal (Al), 230 is a layer of TiN, 240 is another layer of metal (Al) and layer 250 is a layer of TiN/Ti. None of these "layers" is the "final layer" as defined in the present application as the layer of metal associated with the process of manufacturing pads that provide electrical contacts to outside the semiconductor device being manufactured [A copy of the pertinent Xing et al. drawings is in the Appendix]. Xing et al. divides the layer of interconnect material into two layers (210 & 240) separated by a layer of TiN so that in later processes air gaps are formed between adjacent interconnects in order to reduce capacitance. During the manufacturing of pads it is necessary to completely remove the layer of TiN during**

pad etch so it will not interfere with the gold wire bonding process. Because Xing et al. leaves a layer of TiN (230), Xing et al. is not concerned with the "final layer" of metal as is the present invention. The gold wire bonding process is not contemplated in Xing et al. because Xing et al. is concerned with the manufacture of interconnects.] on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal **[the layer 210 IS NOT THE "FINAL" LAYER OF METAL AS DESCRIBED ABOVE]**; forming a first layer of photoresist (200) on the layer TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of interlayer, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaining portions of the layer of TiN (see figure 2C) **[THE EXAMINER IS IN ERROR—THE REMAINING PORTIONS OF TiN ARE NOT REMOVED, THE LAYERS (UNNUMBERED IN FIGURE 2C) OVER STRUCTURES 240 ARE TiN AND HAVE NOT BEEN REMOVED—NOTE THAT THE UNNUMBERED LAYERS, WHICH ARE TiN, REMAIN IN FIGURE 2D—IN ADDITION, XING ET AL. DOES NOT REMOVE THE LAYER OF PHOTORESIST AND THE LAYER 205 DURING THE SAME PROCESS AS DOES THE PRESENT APPLICATION]**; and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280). **[XING ET AL. MUST PERFORM AN ADDITIONAL STEP, I.E., REMOVING THE SECOND LAYER 210 OF METAL (Al).]**

Appellants submit that Xing et al. does not anticipate the present invention because:

(1) Xing et al. does not:

form a "final layer of metal" as defined in the present invention on a layer of interlayer dielectric. [Claim 1 & Specification, page 1, lines 15 et seq.]

(2) Xing et al. does not:

remove the first layer of photoresist and the remaining portions of the layer of TiN in the same process. [Claim 1 & Specification, page 5, lines 28 & 29]

(3) Xing et al. does not:

pattern and develop the second layer of photoresist exposing portions of the blanket layer of interlayer dielectric overlying metal structures, (i.e., where the "pads" will be formed). [Claim 3]

(4) Xing et al. does not:

etch the exposed portions of the blanket layer of interlayer dielectric down to the metal structures. [Claim 3] There are no "metal structures" in Xing et al. on which "pads" are to be formed because Xing et al. is not concerned with the "final" layer of metal on which pads are to be formed.

(5) Xing et al. does not:

etch the first layer of photoresist and the layer of TiN by a process utilizing fluorine containing gas chemistry at an elevated temperature. [Claim 5 & Specification, page5, lines 29 et seq.]

The Examiner has confused "apples with oranges" in the rejection and the rationale for the rejection. Xing et al. describe a series of processes in the manufacture of a semiconductor device and the applicants describe a completely different series of processes in the manufacture a semiconductor device [it could be the same semiconductor device]. The series of processes described in Xing. et al. provide: "An ultimate low k (k = 1) gap structure for high speed logic devices in which the sidewalls fully or partially cover the gaps between the interconnects by dry etching the already formed aluminum interconnects after the photoresist has been stripped. This method is particularly useful for the subsequent deposition of silicon dioxide and for forming air gaps."

The series of processes described in the present invention provide a method of forming pads that provides increased throughput because the layer of TiN has been completely removed in the same process that removes the layer of photoresist.

In view of the above, because Xing et al. does not anticipate the present invention, the rejection of Claim 1 by the Examiner under 35 U.S.C. §102 (e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026) was not proper.

ISSUE 2. Is the rejection of Claims 1 and 3 – 5 under 35 U.S.C. §103 (a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art proper?

The Examiner rejected Claims 1, 3-5 under 35. U.S.C. §103(a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art. The Examiner stated:

> Referring to figures 1-3D, Xing et al. teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) **[This statement is incorrect and indicates that the Examiner does not understand the teachings of Xing et al. Layer 210 is a layer of metal (Al), 230 is a layer of TiN, 240 is another layer of metal (Al) and layer 250 is a layer of TiN/Ti. None of these "layers" is the "final" layer as defined in the present application is the layer of metal associated with the process of manufacturing pads that provide electrical contacts to outside the semiconductor device being manufactured. [A copy of the pertinent Xing et al. drawings is in the Appendix] Xing et al. divides the layer of interconnect material into two layers (210 & 240) separated by a layer of TiN so that in later processes air gaps are formed between adjacent interconnects in order to reduce capacitance. During**

the manufacturing of pads it is necessary to completely remove the layer of TiN during pad etch so it will not interfere with the gold wire bonding process. Because Xing et al. leaves a layer of TiN (230), Xing et al. is not concerned with the "final layer" of metal as is the present invention. The gold wire bonding process is not contemplated in Xing et al. because Xing et al. is concerned with the manufacture of interconnects.] on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal **[the layer 210 IS NOT THE "FINAL" LAYER OF METAL AS DESCRIBED ABOVE]**; forming a first layer of photoresist (200) on the layer TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of interlayer, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaining portions of the layer of TiN (see figure 2C) **[THE EXAMINER IS IN ERROR—THE REMAINING PORTIONS OF TiN ARE NOT REMOVED, THE LAYERS (UNNUMBERED IN FIGURE 2C) OVER STRUCTURES 240 ARE TiN AND HAVE NOT BEEN REMOVED—NOTE THAT THE UNNUMBERED LAYERS, WHICH ARE TiN, REMAIN IN FIGURE 2D—IN ADDITION, XING ET AL. DOES NOT REMOVE THE LAYER OF PHOTORESIST AND THE LAYER 205 DURING THE SAME PROCESS AS DOES THE PRESENT APPLICATION]**; and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280). **[XING ET AL. MUST PERFORM AN ADDITIONAL STEP, I.E., REMOVING THE SECOND LAYER 210 OF METAL (Al).]**

The Examiner admitted, however, that:

> However, the reference does not teach depositing a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer, etching the photoresist layer and TiN layer by using fluorine containing gas chemistry at an elevated temperature.

The Examiner continued:

> Referring to figures 1A-1I, the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, patterning and developing the first layer of photoresist exposing portions of the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer, removing the first layer of photoresist and the layer of TiN **[This is untrue, the layer 106 of TiN is not removed, see Figs. 1E, 1F, 1G 1H & 1I, WHICH CLEARLY SHOW LAYER 106 OF TiN HAS NOT BEEN REMOVED]**, depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric overlying metal structures; and etching the exposed portion of the blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1A-1I of the Admitted Prior art and related text).

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The Examiner then concluded:

> Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time the invention was made would form a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to expose the metal layer as taught by the Admitted Prior art in process of Xing et al. because the technique is known in manufacturing a semiconductor device.

Applicants have pointed out that the Examiner has made an error in the interpretation of Xing et al. and as even more apparent, no matter how the disclosure and teaching of Xing et al. is combined with what the Examiner has termed the "Admitted Prior Art" the claimed invention is not disclosed, taught or suggested. In addition, the Examiner somehow did not realize that the layer **106** of TiN has not been removed from the prior art process.

The Examiner also stated:

> The examiner takes Official Notice that the embodiment described in claim 5 would have been obvious to skilled worker in the art at the time the invention was made because determining the optimum material for etching the layer only involved routine skill in the art (see MPEP 2144.03).

The Examiner's Official Notice is meaningless because nowhere in the application is it stated or suggested that the material used for etching was the "optimum" material. The inventors have invented a way to "simultaneously remove photoresist and the layer of TiN" using a particular material. If the Examiner wishes to reject Claim 5, the Examiner is required to find a reference that either uses the claimed material or suggests the use of the claimed material or any material that removes the layer of photoresist and the layer TiN in the same process.

In addition, the use of the so-called Applicants' Admitted Prior Art by Examiner as a §103 reference is inappropriate. Appellants discussed a method of forming pads as known by the Appellants that was used in the prior art because they were conscientious in their duty of disclosure. Appellants pointed out specifically the drawbacks in the prior art, specifically the decrease in throughput caused by the necessity of etching the layer of TiN. Appellants therefore invented a method to avoid the necessity of separately etching the layer of TiN when the pads were being formed. The Examiner then apparently used this discussion as "a suggestion" under the requirements of §103 to conclude that the invention was "obvious." This is inappropriate and will "chill" the

willingness of applicants to disclose processes used "in house" for which applicants have invented solutions for problems.

The semiconductor manufacturing industry expends many millions of dollars in research and development to find improvements in the manufacture of semiconductors and how the semiconductor devices function. Each such improvement comes at the expense of time and money by the semiconductor manufacturer and after many hours of testing and evaluation. The semiconductor manufacturers certainly do not expend all of these resources needlessly on "obvious" inventions. For an Examiner to conclude, without any objective evidence, that something "would be obvious" is egregious and is considered so by the semiconductor industry. In addition, for the Examiner to make a conclusion based upon a mistaken interpretation of one of the cited references is especially egregious.

The judicially established standard for a finding of obviousness is that: "There must be some reason suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge cannot come from the applicant's invention itself. In re Oetiker, 977 F.2d 1443, 1447 (Fed. Cir. 1992) *citing* Diverstech Corp. v. Century Steps, Inc. 850 F.2d 675, 678-9 (Fed. Cir. 1988).

Furthermore, the Federal Circuit has made it clear that: "The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. *See In re Piasecki,* 745 F.2d 1468, 1471-1472 (Fed. Cir. 1984). It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F. 2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988) *citing* In re Lalu, 747 F. 2d 703, 705 (Fed. Cir. 1984).

Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ACS Hosp sys. [Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 (Fed. Cir. 1984). [emphasis added] And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." In Re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988). [emphasis added]

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The critical inquiry is whether "there is something in the prior art as a whole *to suggest* the desirability, and thus the obviousness of making the combination." Fromson v. Advance Offset Plate, Inc., 755 F.2d 1549, 1556 (Fed. Cir. 1985) *quoting* Lindemann Maschinenfabric GMBH v. American Hoist & Derrick Co., 730 F.2d 1453 (Fed. Cir 1984).

It is apparent that the Examiner did not comply with the above-quoted standards established mainly by the Federal Circuit. The question is WHY didn't the Examiner complied with standards and why doesn't the Applicants have the right to expect that their application will be examined by the standards established by the Federal Circuit. Appellants are convinced that the present application has been examined and rejected based upon unsubstantiated subjective opinions of the Examiner.

In view of the above, the rejection of Claims 1 and 3 – 5 under 35 U.S.C. §103 (a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art was not proper.

ISSUE 3 Was it proper for the Examiner to refuse to enter the proposed amendment on the ground that the "new limitation 'simultaneously' in claim 1 contain the new subject matter that would require further consideration/search" in view of the fact that the specification contains the language: "The layer 108 of photoresist and the layer 106 of TiN are stripped during the same process step."

Because the specification contained the statement: "The layer **108** of photoresist and the layer **106** are stripped during the same process step," Appellants submit that the refusal by the Examiner to enter the proposed amendment was improper.

IN SUMMARY appellants believe that the rejections by the Examiner and the refusal of the Examiner to enter the proposed amendment are improper.

Respectfully submitted,

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APPENDIX
CLAIMS ON APPEAL

1. A method of manufacturing a semiconductor device, wherein the method comprises:

forming a final layer of metal on a layer of interlayer dielectric in the semiconductor device;

forming a layer of TiN on the final layer of metal;

forming a first layer of photoresist on the layer of TiN;

patterning and developing the first layer of photoresist exposing portions of the interlayer dielectric, wherein metal structures are formed;

removing the first layer of photoresist;

removing remaining portions of the layer of TiN; and

forming a blanket layer of interlayer dielectric on the surface of the semiconductor device.

3. The method of Claim 1 further comprising:

forming a second layer of photoresist on the blanket layer of interlayer dielectric;

patterning and developing the second layer of photoresist exposing portions of the blanket layer of interlayer dielectric overlying metal structures; and

etching the exposed portions of the blanket layer of interlayer dielectric overlying metal structures; and

etching the exposed portions of the blanket layer of interlayer dielectric down to the metal structures.

4. The method of Claim 3 further comprising removing the second layer of photoresist.

5. The method of Claim 1 wherein the first layer of photoresist and the layer of TiN is etched by a process utilizing fluorine containing gas chemistry at an elevated temperature.

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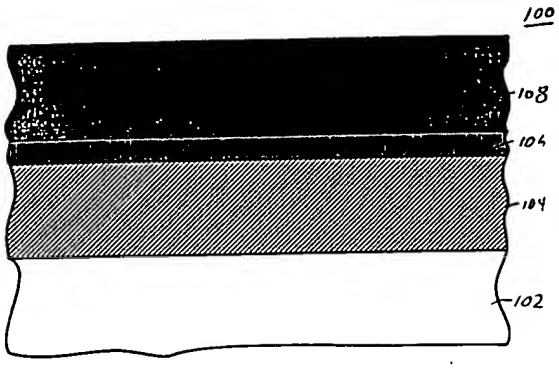

FIGURE 1A (PRIOR ART)

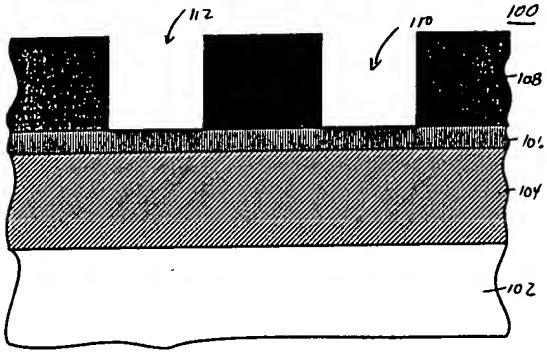

FIGURE 1B (PRIOR ART)

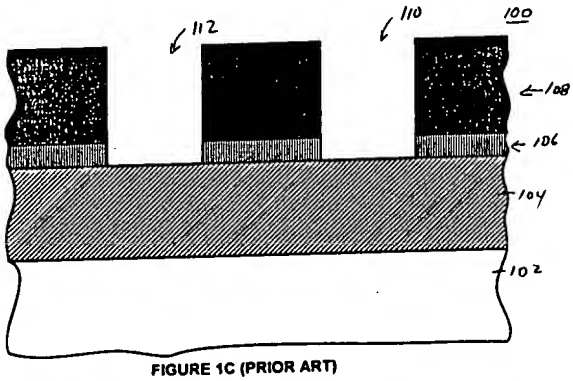

FIGURE 1C (PRIOR ART)

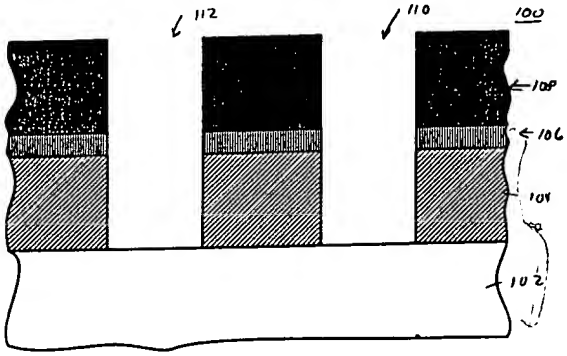

FIGURE 1D (PRIOR ART)

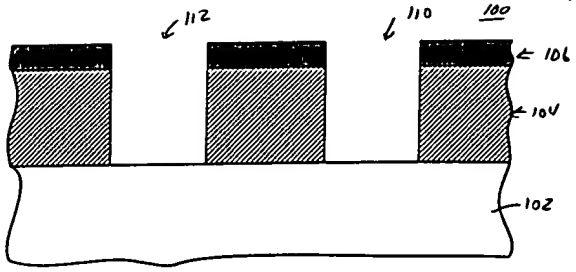

FIGURE 1E (PRIOR ART)

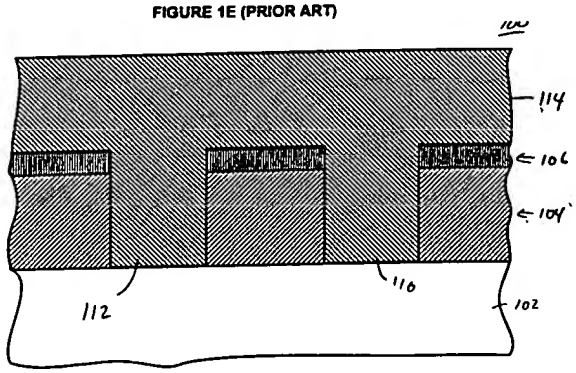

FIGURE 1F (PRIOR ART)

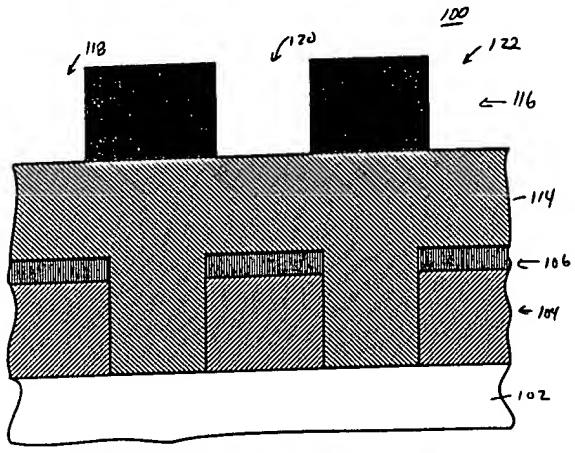

FIGURE 1G (PRIOR ART)

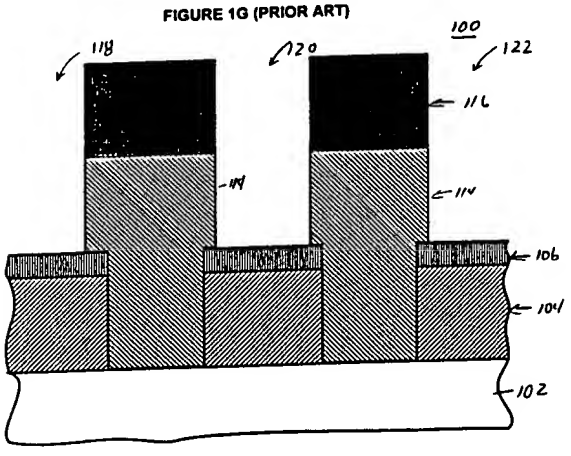

FIGURE 1H (PRIOR ART)

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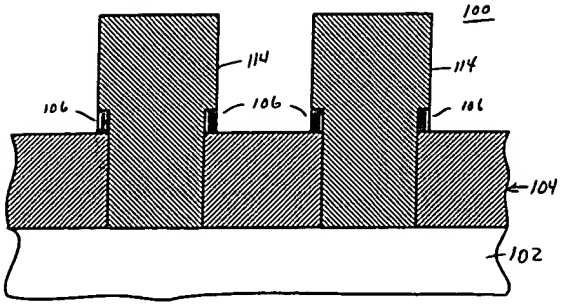

FIGURE 1I (PRIOR ART)

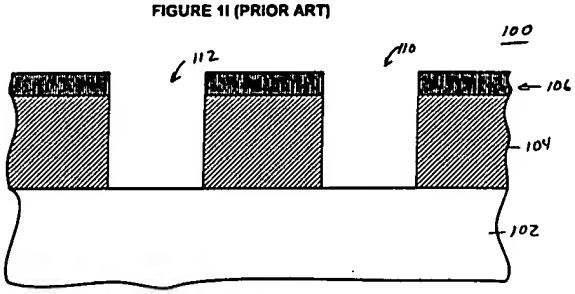

FIGURE 2A

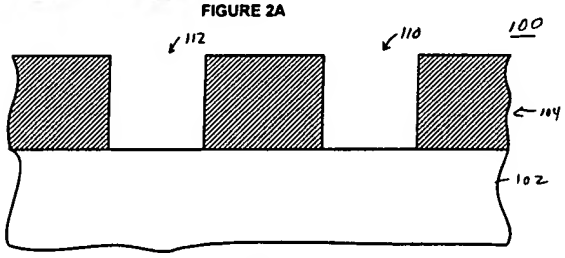

FIGURE 2B

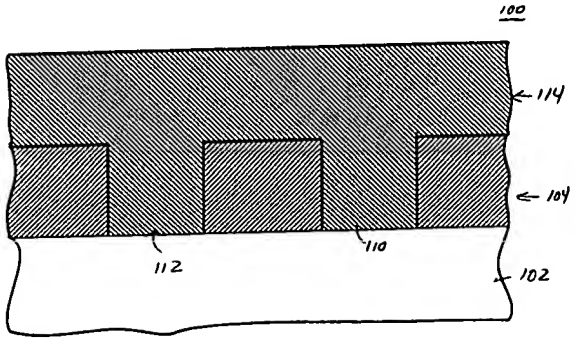

FIGURE 2C

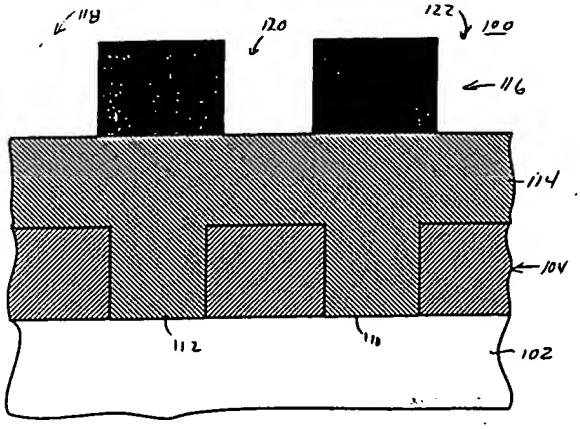

FIGURE 2D

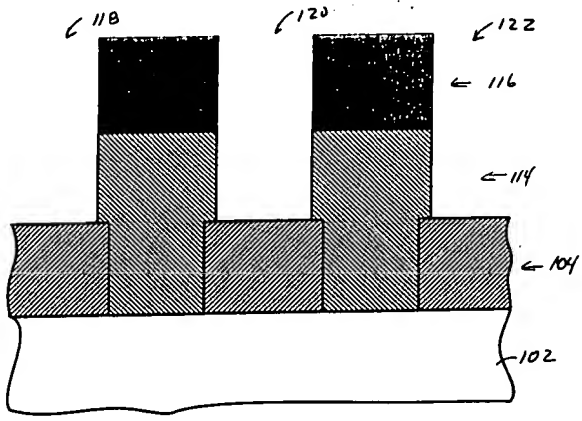

FIGURE 2E

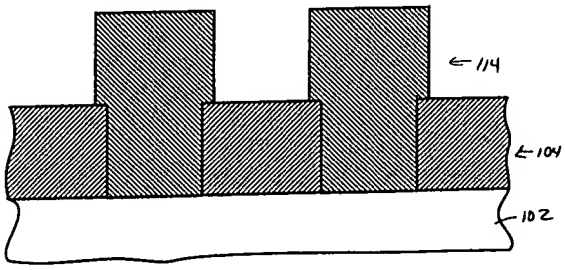

FIGURE 2F

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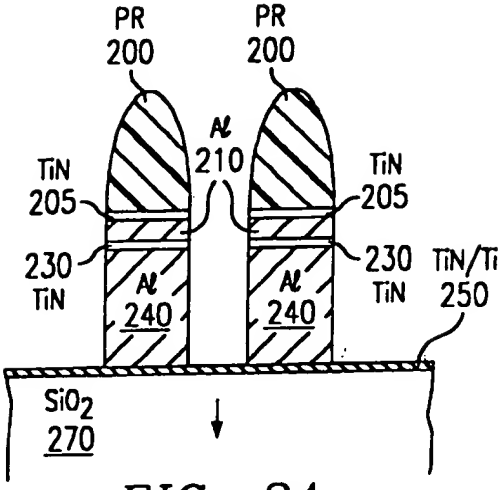

FIG. 2A

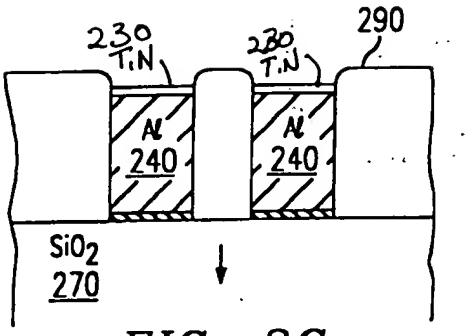

FIG. 2C

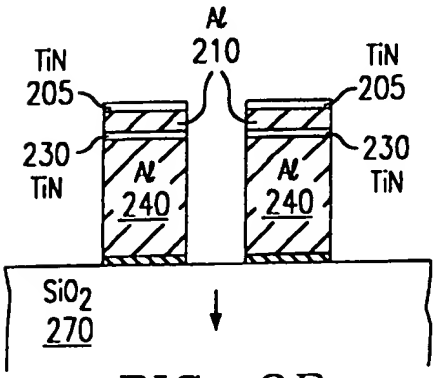

FIG. 2B

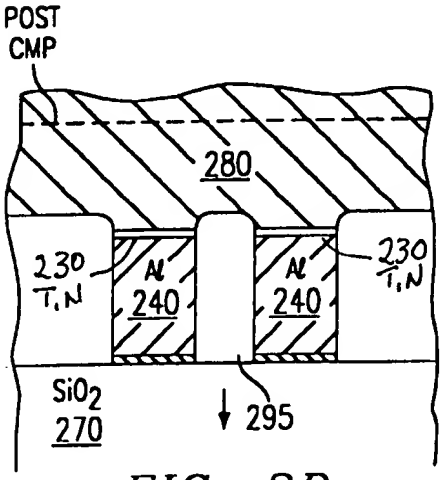

FIG. 2D

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Signature

H. DONALD NELSON
Typed or printed name

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AF

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. D730 / 2813

In Re Application Of: **Shields & Ko**

Serial No.	Filing Date	Examiner	Group Art Unit
09/208,325	12/9/98	T. Nguyen	2813

Invention: **A SACRIFICAL TiN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **12/13/00**

The fee for filing this Appeal Brief is: **$310.00**

☐ A check in the amount of the fee is enclosed.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **01-0365**
A duplicate copy of this sheet is enclosed.

H Donald Nelson
Signature

Dated: **2/13/01**

H. Donald Nelson, Reg. No. 28,980

I certify that this document and fee is being deposited on **2/13/01** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

H Donald Nelson
Signature of Person Mailing Correspondence

H. Donald Nelson
Typed or Printed Name of Person Mailing Correspondence

cc: